REMARKS

Claims 1-34 are pending, with claims 1, 8, 11, 16, 21, 25 and 33 being independent. Claims 11, 16, 21, 25 and 33 have been amended. No new matter has been added. Reconsideration and allowance of the above-referenced application are respectfully requested.

Objection to the Specification

The title stands objected to as allegedly being not descriptive. Although the original title is correct and descriptive, a new title has been provided. Thus, withdrawal of the objection to the specification is respectfully requested.

Claim Rejections under 35 U.S.C. 101

Claims 16-20 stand rejected under 35 U.S.C. 101 as allegedly directed to potentially non-statutory subject matter. The preamble of independent claim 16 has been amended as suggested in the Office Action. In view of this, withdrawal of the rejection of claims 16-20 under 35 U.S.C. 101 is respectfully requested.

Claim Rejections under 35 U.S.C. 102

Claims 11, 12, 15-17 and 20 stand rejected under 35 U.S.C. 102(b) as allegedly being anticipated by Rajwar (Speculative Lock Elision). This contention is respectfully traversed.

Independent claims 11 and 16 each recite, "effecting synchronization between the parallel processes using processor speculation in the data processing machine[.]" Thus, processor speculation is used to bring about synchronization between the parallel processes. In stark contrast, Rajwar describes systems and techniques for avoiding synchronization altogether.

Rajwar describes lock elision (i.e., omission) using speculation. Rajwar explicitly states that, "Synchronization instructions are predicted as being unnecessary and elided. [...] Successful speculative elision is validated and committed without acquiring the lock." (See Rajwar at Abstract, page 294, col. 1; emphasis added.) Rajwar dynamically removes the synchronization locks around critical sections, and then performs critical sections speculatively. The process is summarized by Rajwar as follows:

> In this paper, we show how hardware techniques can be used to remove dynamically unnecessary serialization from an instruction stream and thereby increase concurrent execution. In Speculative Lock Elision

> (SLE), the hardware dynamically identifies synchronization operations, predicts them as being unnecessary, and elides them. By removing these operations, the program behaves as if synchronization were not present in the program. Of course, doing so can break the program in situations where synchronization is required for correctness. Such situations are detected using pre-existing cache coherence mechanisms and without executing synchronization operations.

(See Rajwar at Section 1, page 295, col. 1; emphasis added.) Thus, independent claims 11 and 16 should be allowable for at least the reason that claims 11 and 16 require effecting synchronization, while Rajwar attempts to avoid synchronization.

Nonetheless, claims 11 and 16 have been amended to clarify the claimed subject matter and now recite, "effecting synchronization between the parallel processes using processor speculation in the data processing machine to speculatively read-modify-write a lock variable associated with a critical section[.]" (Emphasis added.) Support for this amendment can be found throughout the application as filed, such as the detailed description corresponding to Figure 5 of the patent application. This amendment makes clear that the speculative execution is of the lock acquisition code, not merely the

critical section as done in Rajwar. Thus, for all of the above reasons, independent claims 11 and 16 should be in condition for allowance. Dependent claims 12, 15, 17 and 20 should be patentable based on the above arguments and the additional recitations they contain.

Claim Rejections under 35 U.S.C. 103

Claims 1, 6, 7, 14, 19, 21-27 and 31-34 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Rajwar in view of Lam (Enhancing Software Reliability with Speculative Threads). Claims 2-5 and 8-10 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Rajwar/Lam in view of Christie (U.S. 6,009,512). Claims 13, 18 and 28 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Rajwar in view of "common prior art." Claims 29 and 30 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Rajwar/Lam in view of "common prior art." These contentions are respectfully traversed.

The Official Action asserts that Lam discloses, "an instruction set architecture including speculative execution control circuitry that handles at least one machine instruction that facilitates synchronization between parallel processes by

exposing the processor speculation to program control (Lam page 187 TRY instruction)." (*See* Office Action mailed May 4, 2006, at pages 5-6.) However, contrary to this assertion, Lam does not teach synchronization between parallel processes.

Lam describes techniques to enhance the reliability of software through the use of monitoring programs executed speculatively in parallel with the main program being monitored. (*See* Lam throughout.) A monitoring program is additional code introduced to the main program to monitor whether the main program is behaving correctly and to recover from errors. (*See* Lam at Section 1.) By definition, a monitoring program does not need to synchronize with the main program because the two programs do not need to coordinate their accesses to a shared resource. As described in Lam, "Monitoring functions need to observe the main program's state, but unless anomalies are detected, they do not have any effect on the execution of the main program." (*See* Lam at Section 1.1; emphasis added.)

Furthemore, a prima facie case of obviousness has not been established because there is no motivation to combine Rajwar with Lam as suggested by in the Office Action. The Official Action suggests that Rajwar would be motivated to use the instructions of Lam to effect synchronization. (*See* Office

Action mailed May 4, 2006, at page 6.) However, this suggestion directly contradicts Rajwar's own teachings.

Rajwar's explicit purpose is to not expose the speculative execution to program control by the user.

> Ideally, programmers would be able to use frequent and conservative synchronization to write obviously correct multithreaded programs, and a tool would automatically remove all such conservative use. Thus, even though programmers use simple schemes to write correct code, synchronization would be performed only when necessary for correctness; [...] SLE can be implemented entirely in the microarchitecture, without instruction set support and without system level modifications (e.g., no coherence protocol changes are required) and is transparent to programmers. Existing synchronization instructions are identified dynamically. Programmers do not have to learn a new programming methodology and can continue to use well understood synchronization routines.

(*See* Rajwar at Section 1, page 295, cols. 1 & 2; emphasis added.) Thus, Rajwar actually teaches away from the proposed combination.

Moreover, even if Rajwar and Lam were combined, the result would not be the presently claimed subject matter. Lam teaches the use of instructions that facilitate monitoring of main

programs through speculative, parallel execution of monitoring programs. Rajwar teaches the use of speculative execution of critical sections in parallel processes after determining that explicit synchronization is unnecessary. Neither reference (either alone or in combination) teaches or suggests exposing processor speculation to program control to facilitate synchronization between parallel processes.

For all of the above reasons, a prima facie case of obviousness has not been established for any of independent claims 1, 8, 21, 25 and 33. Dependent claims 2-10, 12-15, 17-24, 26-32 and 34 should be patentable based on the above arguments and the additional recitations they contain.

Nonetheless, independent claims 21, 25 and 33 have been amended, in a manner similar to independent claims 11 and 16, to clarify that the speculative execution is a speculative read-modify-write of a lock variable associated with synchronizing access to a critical section, as opposed to merely speculatively executing the entire critical section. This is in stark contrast with Rajwar, where the entire critical section is speculatively executed and the lock acquisition is avoided entirely. As described in Rajwar:

> To our knowledge, this is the first proposed technique for removing dynamically unnecessary and conservative synchronization operations from a dynamic execution without performing the lock-acquire and release operations, and without requiring exclusive ownership of the lock variable.

(See Rajwar at Section 1, page 295, col. 2; emphasis in original.)

By speculatively executing the lock acquisition, resource constraints can be avoided. For example, some critical sections are so long, if the entire critical section were executed speculatively, the processor's buffer size might be exceeded. In contrast, by speculatively executing the lock acquisition, synchronization between parallel processes can be implemented while also reducing the number of processor cycles needed to acquire the lock before entering the critical section.

Conclusion

It is believed that all of the pending claims have been addressed. However, the absence of a reply to a specific issue or comment does not signify agreement with or concession of that issue or comment. Because the arguments made above may not be exhaustive, there may be reasons for patentability of any or all

pending claims (or other claims) that have not been expressed. Finally, nothing in this paper should be construed as an intent to concede any issue with regard to any claim, except as specifically stated in this paper, and the amendment of any claim does not necessarily signify concession of unpatentability of the claim prior to its amendment.

It is respectfully suggested for all of these reasons, that the current rejections are overcome, that none of the cited art teaches or suggests the features which are claimed, and therefore that all of these claims should be in condition for allowance. A formal notice of allowance is thus respectfully requested.

No fees are believed due with this response. Please apply any necessary charges or credits to deposit account 06-1050.

Respectfully submitted,

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